Si-SiO_2 Composite MEMS Resonators in CMOS Compatible Wafer-scale Thin-Film Encapsulation

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***Abstract*— Si-SiO_2 composite resonators in wafer-scale thin-film encapsulation are demonstrated. These resonators are fabricated in hermetic wafer-scale thin-film encapsulation, which enables mass production with high yield even after harsh post processes. Also this encapsulation provides potential for integration of frequency references with CMOS circuitry. The encapsulated composite resonators exhibit tunable temperature dependence of resonant frequency with a high quality factor of much larger than 10,000. Up to 40x improvement in temperature stability was demonstrated.**

I. INTRODUCTION

Quartz resonators have many unbeatable advantages in size, price, and power consumption. Therefore quartz oscillators are still dominating the current billion-dollar frequency reference market, even though several alternative frequency references have been suggested such as atomic clocks or GPS clocks.

However, attention has been being drawn to silicon based resonators. Silicon resonators fabricating lithography based technology have many significant benefits including reduction both in size and cost. In addition fabricating frequency references with their corresponding circuit components seemed plausible. But in spite of such many potential benefits, still replacement of current dominant quartz crystal oscillator has not been easy. The performance requirement of MEMS resonators as a frequency reference is strict. In particular, stability against time and temperature has been the most critical problem.

Recently, silicon resonators packaged in a controlled environment demonstrated commercial level long-term stability [1]. The silicon resonators were packaged by 'epi-seal' encapsulation process, which is a wafer-scale thin-film encapsulation using epitaxial silicon deposition at CMOS clean high temperature (~1000°C). 'Epi-seal' eliminated, or at least minimized, most of the potential aging mechanisms of silicon resonators, such as contamination-decontamination process, pressure change, and diffusion effects.

However, unlike long-tem stability, temperature stability requires further improvement. Silicon has inherent characteristic hat becomes softer as temperature increases. Therefore, without some form of compensation of environmental temperature changes, resonant frequency of silicon based resonators is not stable enough as a frequency reference. Thus many approaches have been suggested to overcome this change in stiffness of silicon [2-6].

One approach is compensating the environmental temperature change with a feedback loop [2, 3]. However this approach requires several additional components including temperature sensors, control circuitry, and compensator. Thus increase in size or complexity of the oscillator is not avoidable in case of these kinds of compensation approach.

The other approach is introducing one or more number of materials, other than silicon, and utilizing the difference in their mechanical properties [4-6]. Many of them use thermal expansion mismatch between silicon and the compensating materials, which were mostly metal (gold or aluminum). However, gold or aluminum itself exhibits mechanical instability, such as fatigue and hystersis, therefore, again long-term stability of this approach can be problematic.

Recently Shen et al, suggested using composite materials to reduce thermal drift for silicon cantilever [7]. If a silicon resonator is compensated with a material that becomes stiffer as temperature increases, such as silicon dioxide, it may be possible to overcome the material softening effect in silicon.

Using Si- SiO_2 for temperature compensation is promising because both materials are the two most common materials in MEMS or CMOS fabrication process. This approach doesn't require additional power or increase in size or control circuit. Also, it seems plausible to encapsulate these materials with minor modification in the 'epi-seal' encapsulation, of which benefits for MEMS resonators are already demonstrated such as

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high yield of devices on completed wafers, reduced package size, and robustness against harsh post processing. In addition, hermetic vacuum encapsulation will minimize damping through collision with air molecules, thus high quality factor can be achieved for long-term operation [8].

II. Theory and Design

The natural frequency of a transversely vibrating flexure beam can generally be expressed as,

$$f_i = \frac{\lambda_i}{2\pi L^2}\sqrt{\frac{EI}{\rho A}}; \quad i = 1,2,3\cdots, \tag{1}$$

where λ_i is the mode constant for a beam with particular boundary conditions, L is the length of the beam, and ρ is the density of the beam, A is the cross sectional area, E is Young's modulus of the material, and I is the moment of inertia of the beam cross section about the neutral axis.

The temperature coefficient of natural frequency (TCf) can be defined as,

$$TCf = \frac{1}{f}\frac{df}{dT} = \frac{1}{2}\frac{1}{EI}\frac{d(EI)}{dT} \tag{2}$$

assuming the effect of dimensional change due to thermal expansion is negligible.

In case of composite beams with a uniform cross-section along the length, the natural frequency can be computed using the same formula by defining the composite beam equivalent stiffness,

$$EI = \sum_k E_k I_k \tag{3}$$

Therefore, TCf for composite resonator can be defined as follows

$$TCf = \frac{1}{2}\frac{\sum_k E_k I_k TCE_k}{\sum_k E_k I_k} \tag{4}$$

where, TCE(Temperature dependence of Young's modulus) is defined as,

$$TCE = \frac{1}{E}\frac{dE}{dT} \tag{5}$$

The material properties of silicon and silicon dioxide used are summarized in Table I.

TABLE I. Material properties of silicon and silicon dioxide at around room temperature (30°C) [9]

	E (GPa)	*TCE (ppm/°C)*
Si	165.6	-67.5
SiO_2	73	185

The moment of inertia, I, becomes bigger as farther apart from the neutral axis, therefore configuration depicted in figure 1-a) was considered. With this configuration, SiO_2 even much smaller amount of Silicon dioxide outside can compensate much larger amount of silicon inside. Also silicon dioxide can be easily formed by oxidizing silicon.

The design of MEMS resonators is shown in figure 1 b). Two parallel beams are coupled using two coupling blocks on both ends. One side is anchored to the substrate, but the other side is floating to avoid axial loading from the substrate. The beams were designed to have a length of 200μm and height of 20μm with width varying between 4μm and 8μm. This background theory and design concept is further discussed in [10].

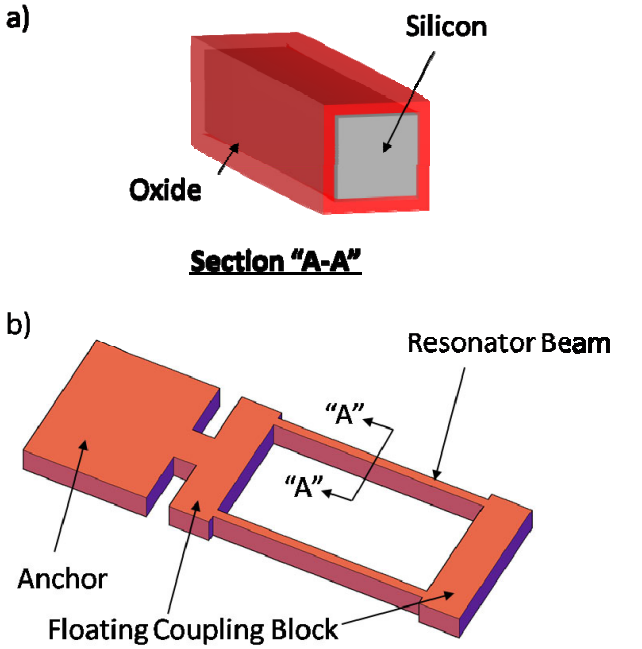

Figure 1 Schematics of Si-SiO_2 composite resonators in this study.

III. Fabrication Process

The Si-SiO_2 composite resonators were fabricated in the modified 'epi-seal' encapsulation [8].

Figure 2 shows the schematic of the fabrication process. The fabrication starts by patterning the resonator structure using DRIE(deep reactive ion etch) leaving 1.5 μm width trenches in a 20μm thick device layer of SOI (silicon on insulator) wafer (step a). Then 2.5μm of silicon dioxide is deposited as a sacrificial layer. This oxide deposition was conducted in four iterations, each of which followed by 1 hour of 1100°C annealing to minimize stress accumulation during deposition. For uniformity, all wafers were rotated 180° at each deposition. This silicon dioxide is stripped off by plasma etch except on top of the devices. Plus small openings are created on top of electrodes for

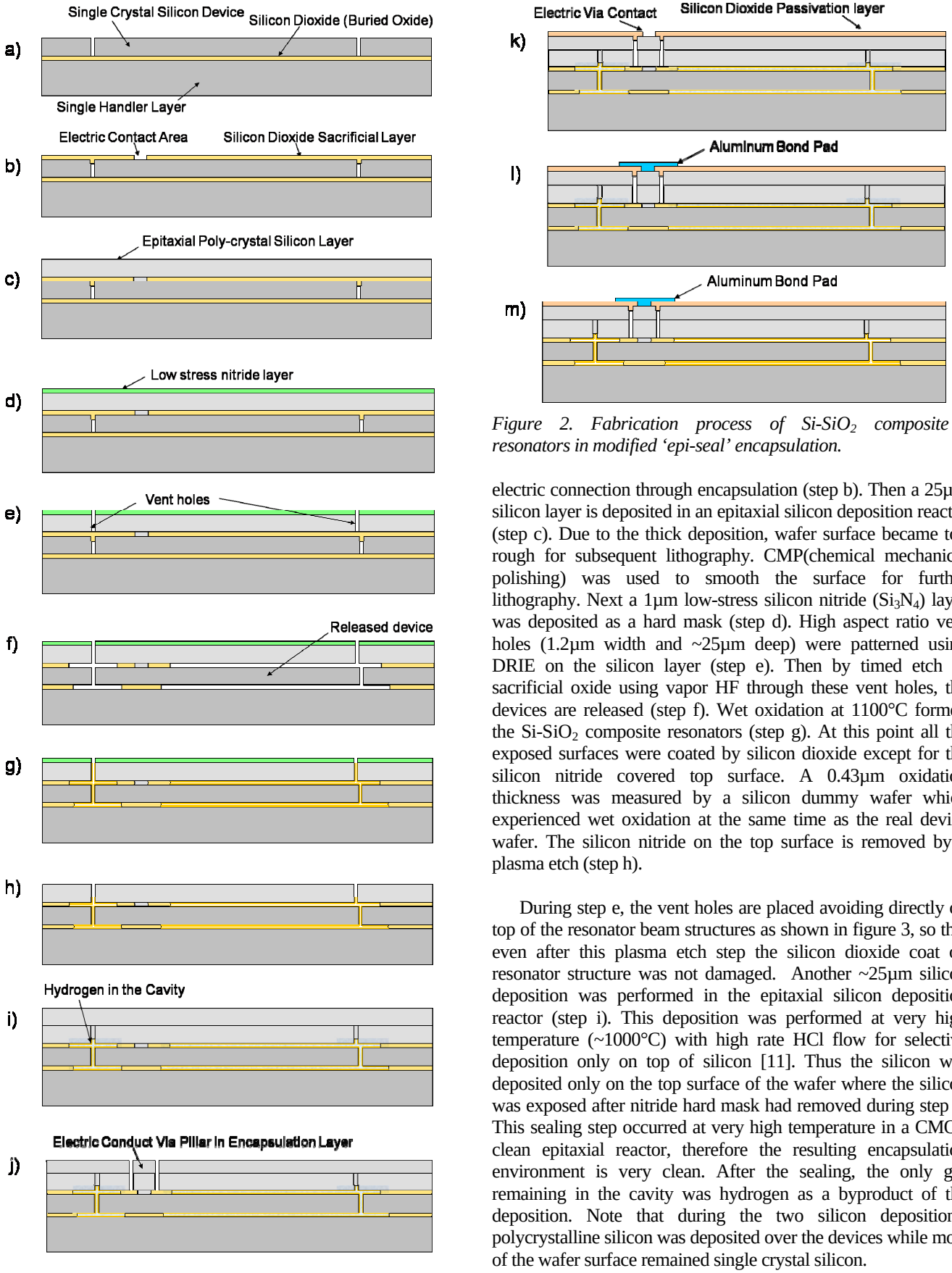

Figure 2. Fabrication process of Si-SiO_2 composite resonators in modified 'epi-seal' encapsulation.

electric connection through encapsulation (step b). Then a 25µm silicon layer is deposited in an epitaxial silicon deposition reactor (step c). Due to the thick deposition, wafer surface became too rough for subsequent lithography. CMP(chemical mechanical polishing) was used to smooth the surface for further lithography. Next a 1µm low-stress silicon nitride (Si_3N_4) layer was deposited as a hard mask (step d). High aspect ratio vent holes (1.2µm width and ~25µm deep) were patterned using DRIE on the silicon layer (step e). Then by timed etch of sacrificial oxide using vapor HF through these vent holes, the devices are released (step f). Wet oxidation at 1100°C formed the Si-SiO_2 composite resonators (step g). At this point all the exposed surfaces were coated by silicon dioxide except for the silicon nitride covered top surface. A 0.43µm oxidation thickness was measured by a silicon dummy wafer which experienced wet oxidation at the same time as the real device wafer. The silicon nitride on the top surface is removed by a plasma etch (step h).

During step e, the vent holes are placed avoiding directly on top of the resonator beam structures as shown in figure 3, so that even after this plasma etch step the silicon dioxide coat on resonator structure was not damaged. Another ~25µm silicon deposition was performed in the epitaxial silicon deposition reactor (step i). This deposition was performed at very high temperature (~1000°C) with high rate HCl flow for selective deposition only on top of silicon [11]. Thus the silicon was deposited only on the top surface of the wafer where the silicon was exposed after nitride hard mask had removed during step h. This sealing step occurred at very high temperature in a CMOS clean epitaxial reactor, therefore the resulting encapsulation environment is very clean. After the sealing, the only gas remaining in the cavity was hydrogen as a byproduct of the deposition. Note that during the two silicon depositions, polycrystalline silicon was deposited over the devices while most of the wafer surface remained single crystal silicon.

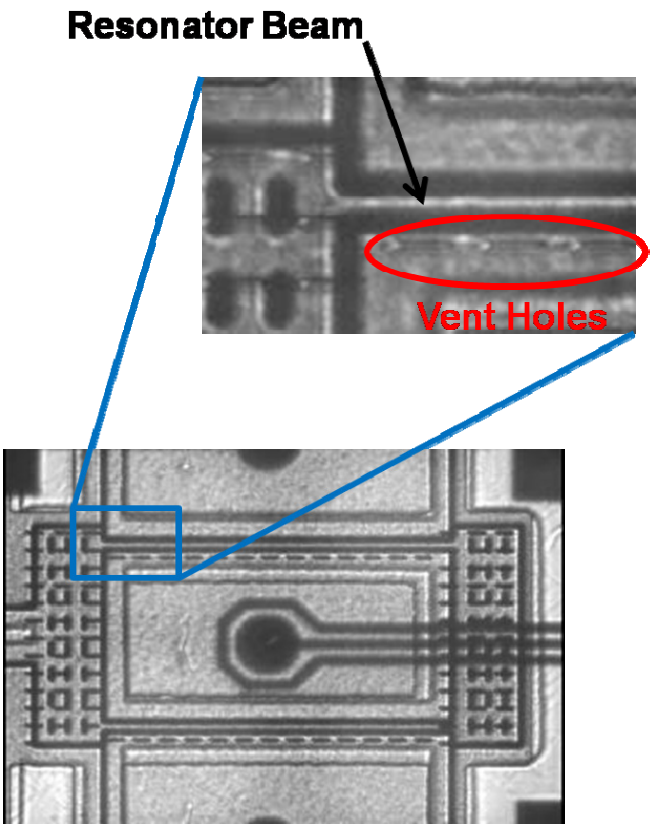

Figure 3. Infrared images of fabricated device. To avoid structure surface damage during plasma etch, vent holes were placed with some offset from the devices.

Again this thick depositions created a rough topology thus, chemical mechanical polishing (CMP) was used to smooth the surface for further lithography.

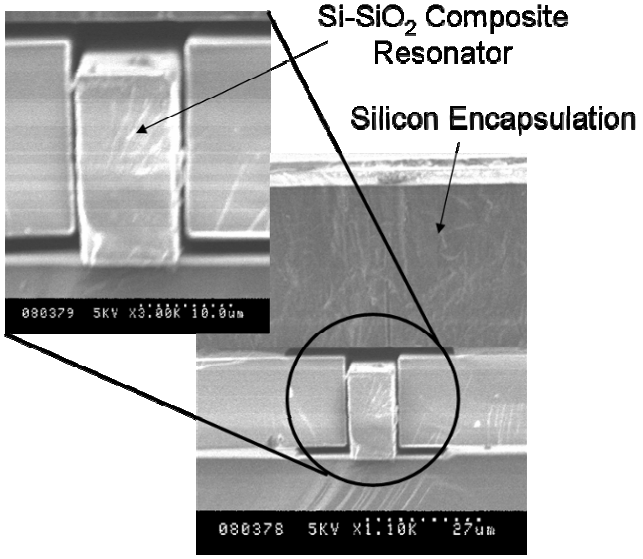

Figure 4. SEM images of cross section of fabricated devices. SiO_2 was uniformly coated around silicon resonator beam by thermal oxidation.

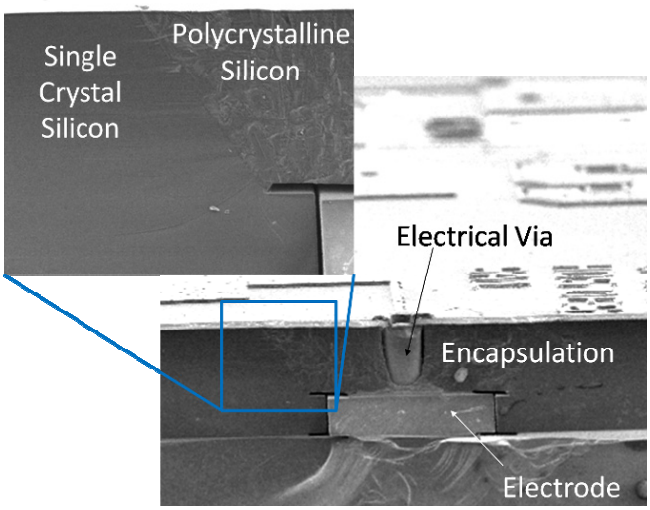

Figure 5. SEM images of cross section of 'epi-seal' encapsulated device. Single crystal silicon and polycrystalline silicon were selectively grown in the encapsulation layer.

The electric via to the device layer was created by etching a pillar into the ~50μm thick silicon encapsulation layer using DRIE (step j). These pillars were connected to the electrodes through the opening erected at step c. Another silicon dioxide layer was deposited as a passivation layer (step k). Next, metal was deposited and patterned for bonding pads and conductive traces (step l). Finally, the wafer was placed in a 400°C nitrogen furnace to diffuse out the hydrogen gas remaining in the cavity (step m). Figure 4 shows a cross section SEM image of fabricated Si-SiO_2 composite resonators in modified 'epi-seal' encapsulation.

During silicon deposition in the epitaxial reactor (step c and step i), single crystal silicon was grown on top of single crystal silicon, whereas polycrystalline silicon was grown on top of sacrificial silicon dioxide deposited at step b (on top of polycrystalline silicon in case of step i) as shown in figure 5. Therefore, most of the wafer surface is left as single crystal silicon where further CMOS fabrication can be possible.

More than 3,000 devices were fabricated on a 4 inch wafer. After fabrication, more than 60 devices were probed, and all those probed were found to work. After dicing into parts using a wafer saw and wire bonded (see figure 6), non-working device had not been found among more than 30 devices that we tested.

All probed devices showed a quality factor of larger than 10,000. This indicates that energy loss due to air damping is minimal. These features are the advantages of using 'epi-seal' encapsulation.

IV. Experiment and Result

Temperature dependence of resonant frequency for these encapsulated Si-SiO_2 composite resonators was examined. Resonators were mounted and wire-bonded in a standard,

Openpak, 8-pin DIP package [12] and installed in a temperature chamber Thermoton S1.2. Using HP4395A network analyzer, resonators were stimulated and the amplified response was measured. The amplifiers used were AD8022A and separately installed outside of the temperature chamber to minimize uncertain temperature effect on the amplifiers. A multiplexer, Agilent 3499B, connected from output of the amplifiers to the network analyzer to monitor up to 10 resonators at a time. By Aglient E3641A power supply, a DC bias was applied to each resonator through another multiplexer.

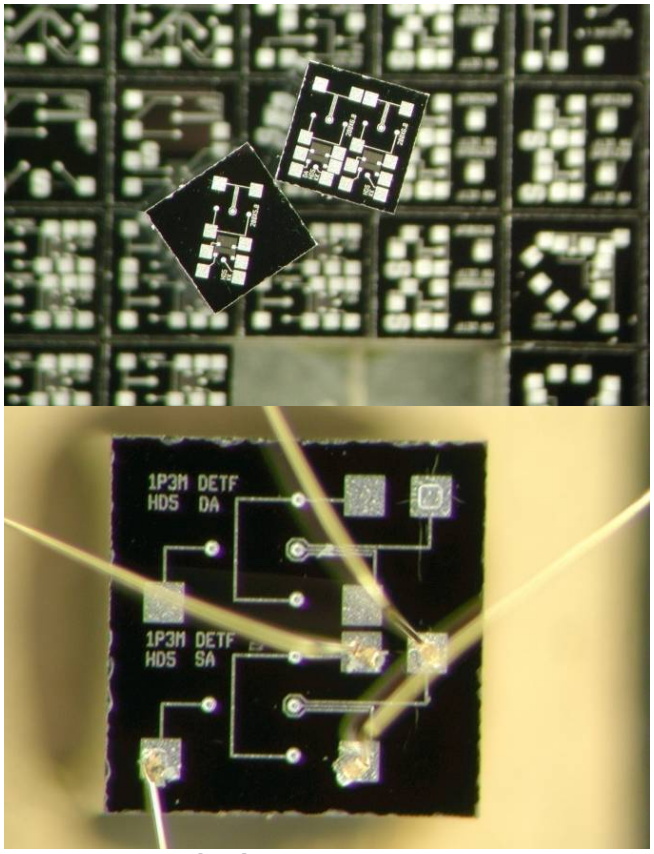

Figure 6. Encapsulated Si-SiO_2 composite resonators were (a) diced into parts and (b) wire bonded for temperature stability experiment.

Figure 7 shows the measured resonant frequency versus temperature. As beam width becomes thinner, the TCf values become more positive. All of the resonators in the test had experienced the same oxidation, thus silicon dioxide layer thickness should be the same as 0.43μm.

Therefore the width of silicon beam determines the ratio between silicon and silicon dioxide thickness. The thicker the relative oxide layer thickness compared to silicon width, TCf becomes more positive. Among the tested devices, the 5.5μm beam resonator exhibits the best temperature stability.

Compared to the pure silicon resonator, it shows more than 10x improvement in TCf, and more than 40x improvement in frequency variation within -15°C to 85°C temperature ranges. The resonant frequencies, TCf, and frequency variations of the tested resonators are summarized in Table II. The small difference between calculated TCf and measured TCf seems to be due to uncertainty in material property values.

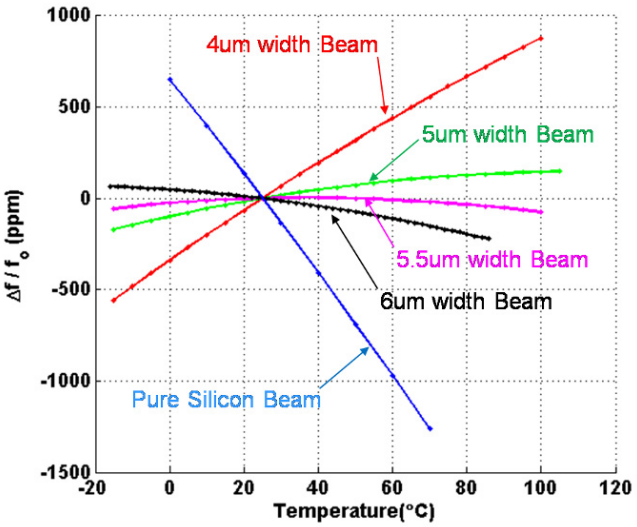

Figure 7. Result of the resonant frequency temperature stability experiment.

V. Conclusion and Future Works

Si-SiO_2 composite resonators were successfully fabricated by thermal oxidation of silicon resonator. More than 3,000 resonators with high yield (>95%) were successfully produced inside CMOS compatible, ultra hermetic wafer-scale encapsulation. Temperature dependence of resonant frequency could be controlled by tuning Si-SiO_2 ratio. Up to 40x improvement in resonant frequency stability against environmental temperature change was demonstrated. This compensation method doesn't involve any additional temperature sensing or control circuitry, thus it doesn't increase size, complexity, or power consumption of the oscillator circuit. Currently, we are pursuing more research on other aspect of Si-SiO_2 composite resonators such as quality factor, long-term stability, and charge trapping for development of commercial level high performance MEMS resonators.

TABLE II. Material Properties of Silicon and Silicon Dioxide at Room Temperature (30°C)

Beam Width (μm)	4	5	5.5	6	Ref.
I_{Ox} / I_{Si}	1.17	0.85	0.74	0.66	0
Frequency (MHz)	0.73	0.94	1.02	1.13	1.31
Q (at 25°C)	~46,000	~26,000	~22,000	~17,000	~10,000
TCf (calculated) (ppm/°C)	10.91	1.87	-1.36	-4.03	-33.8
TCf(measured) (ppm/°C)	12.49	2.63	-0.20	-2.84	-27.34
Frequency Variation (ppm) (-15°C~85°C)	1279.9	301	59.1	279.8	2734.1

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